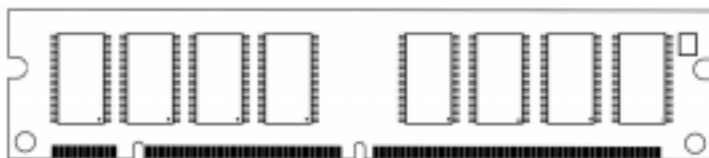


FRONT VIEW



BACK VIEW



GENERAL DESCRIPTION

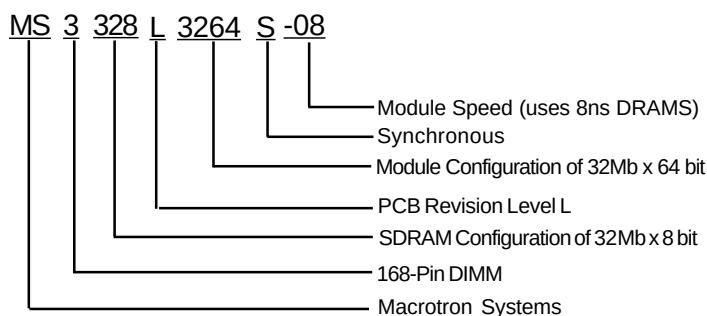
The Macrotron MS3328L3264S-08 is a PC100 Compliant 32M bit x 64 bit Synchronous Dynamic RAM high density memory module. It consists of eight CMOS 32M x 8 bit with Synchronous DRAMs in TSOP packages and a 2K EEPROM in 8-pin TSOP package on a 168-pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The product is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle controls with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- 32 Megabit by 64 bit (256 Megabyte) Synchronous DRAM Module PC 100 Compliant
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 8ns SDRAM components
- Nonbuffered
- Single +3.3V $\pm$ 0.3V power supply
- Fully synchronous; all signals registered on positive edge system clock
- Internal pipeline operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge
- Programmable burst lengths: 1,2,4 or 8
- Auto Precharged and Auto Refresh Modes
- LVTTTL compatible inputs and outputs
- Serial Presence Detect (SPD)

PART NUMBER DESIGNATOR



KEY TIMING PARAMETERS

PARAMETER	VALUE	UNIT
Module Bus Speed	100	MHz
Module Speed	8.0	ns
SDRAM Speed	125	MHz
CAS Latency	2/3	CLOCK
SDRAM Access Time	6.0	ns
SDRAM Setup Time	2.0	ns
SDRAM Hold Time	1.0	ns

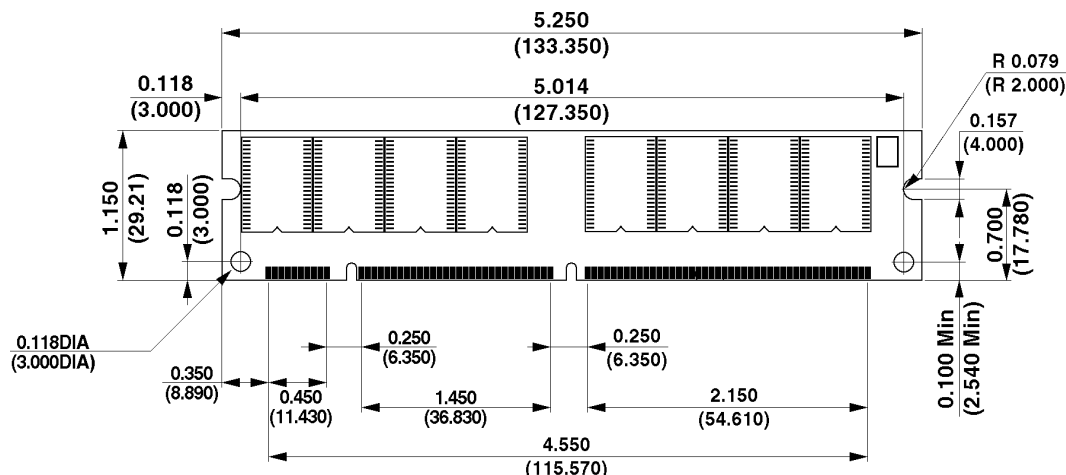


32Mb x 64, 168-Pin DIMM
3.3V Synchronous DRAMs with SPD

PIN NAMES

PIN NAME	FUNCTION
A0~A13	Address Input (multiplexed)
BA0~BA1	Select Bank
DQ0~DQ63	Data Input / Data Output
CLK0~CLK3	Clock Input
CKE0~CKE1	Clock Enable Input
CS0~CS3	Chip Select Input
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
DQMB0~7	DQMB
VDD	Power Supply (3.3V)
VSS	Ground
VREF	Power Supply for Reference
SDA	Serial Data I/O
SCL	Serial Clock
SA0~2	Address in EEPROM
DU	Don't Use
NC	No Connection
AP	Automatic Precharge
WP	Write Protection

****** These pins should be NC in the system which does not support SPD.



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	VALUE	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	C
Power Dissipation	PD	8	W
Short Circuit Current	I_{OS}	50	mA

DC OPERATING CONDITIONS AND CHARACTERISTICS

PARAMETERS		SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage		V_{DD}	3.0	3.6	V	
Input High Voltage (Logic 1), All Inputs		V_{IH}	2.0	$V_{DD} + 0.3$	V	
Input low Voltage (Logic 0), All Inputs		V_{IL}	-0.3	0.8	V	
INPUT LEAKAGE CURRENT Any input $0V \leq V_{IN} \leq V_{DD}$ (All other pins not under test = 0V)	DQMB0~DQMB7	I_{I1}	-10	10	μA	
	CLK0~2, CS0~2#	I_{I2}	-10	10	μA	
	CKE0~1	I_{I3}	-10	10	μA	
	RAS, CAS, A0~A11, BA0~1, WE	I_{I4}	-10	10	μA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; $0V \leq V_{OUT} \leq V_{DD}$)		I_{OZ}	-10	10	μA	
OUTPUT LEVELS						
Output High Voltage		V_{OH}	2.4			$I_{OH} = -2mA$
Output low Voltage		V_{OL}		0.4	V	$I_{OL} = 2mA$

CAPACITANCE ($V_{DD} = 3.3V$, $T_A = 23C$, $F = 1MHZ$, $V_{REF} = 1.4V$)

PARAMETERS	SYMBOL	MAX	UNIT
Input Capacitance ($A_0 \sim A_n$, BA0~1, RAS, CAS, WE)	C_{I1}	35	pF
Input Capacitance (CS0~2#)	C_{I2}	24	pF
Input Capacitance (CKE0~1)	C_{I3}	45	pF
Input Capacitance (DQMB0~7)	C_{I4}	10	pF
Input Capacitance (SCL, SA0~2, WP)	C_{I5}	6	pF
Data Input/Output Capacitance (DQ0~63, SDA)	C_{I0}	10	pF
Input Capacitance (CLK0~3)	C_{I6}	20	pF

OPERATING CONDITIONS AND MAXIMUM LIMITS

PARAMETER/CONDITION	SYMBOL	MAX	UNITS
OPERATING CURRENT: Active Mode, Burst =2 READ or WRITE, $t_{RC} \geq t_{RC} (MIN)$, CAS Latency = 3	ICC1	1130	mA
STANDBY CURRENT: Power-Down Mode, $t_{CK} = 10ns$, $CKE \leq V_{IL} (MAX)$, All banks idle	ICC2	16	mA
STANDBY CURRENT: $CS \geq V_{IH} (MIN)$, $t_{CK} = 10ns$, $CKE \geq V_{IH} (MAX)$, All banks idle	ICC3	48	mA
STANDBY CURRENT: $CS \geq V_{IH} (MIN)$ $t_{CK} = 10ns$, $CKE \geq V_{IH} (MIN)$, all banks active after t_{RCD} met, No accesses in progress	ICC4	560	mA
OPERATING CURRENT: Burst Mode, Continuous burst, READ or WRITE, $t_{CK} = 10ns$, all banks active, Addresses transition once per clock cycle, CAS Latency = 3	ICC5	1060	mA
AUTO REFRESH CURRENT: $t_{RC} > t_{RC} (MIN)$, CAS Latency = 3	ICC6	1860	mA
SELF REFRESH CURRENT: $CKE < 0.2V$	ICC7	40	mA

AC FUNCTIONAL CHARACTERISTICS

PARAMETERS		SYMBOL		UNITS
READ/WRITE command to READ/WRITE command		tCCD	1	tCK
CKE to clock disable or power-down entry mode		tCKED	1	tCK
CKE to clock enable or power-down exit mode		tPED	1	tCK
DQM to input data delay		tDQD	0	tCK
DQM to data mask during WRITES		tDQM	0	tCK
DQM to data high-impedance during READS		tDQZ	2	tCK
WRITE command to input data delay		tDWD	0	tCK
Data-in to PRECHARGE command		tDAL	2	tCK
Data-in to ACTIVE command		tDPL	4	tCK
Last data-in to PRECHARGE command		tRDL	2	tCK
Last data-in to burst STOP command		tBDL	1	tCK
Last data-in to new READ/WRITE command		tCDL	1	tCK
LOAD MODE REGISTER command to command		tMRD	2	tCK
Data-out to high-impedance from PRECHARGE command	CAS latency=3	tROH	3	tCK
	CAS latency=2	tROH	2	tCK

FUNCTIONAL BLOCK DIAGRAM

